

# Statistical Characterization of GaAs E/D HEMT Analog Components for Data Conversion ICs

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## Abstract

Based on the Raytheon model, GaAs E/D HEMT model parameters are measured and their statistical deviations and correlation coefficients are determined. Output current deviations of transistor current sources and DC offset voltages of differential amplifiers, which represent basic limitations of precise data conversion ICs, are characterized using these experimental data and derived equations with seven model parameters. Monte-carlo simulations are carried out on an 8 bit D/A converter and a latched comparator, which were implemented in 0.5  $\mu\text{m}$  GaAs E/D HEMT technology, and simulated results are shown to be identical to measured accuracies of these two circuits.

## Introduction

Semiconductor technologies should provide high precision, high speed and low power dissipation for data conversion ICs. Compared to silicon and GaAs bipolar transistors, submicron GaAs FETs (MESFETs and HEMTs) exhibit a higher operation frequency and a lower power dissipation, thus, some efforts have been made to apply these technologies for realizing high speed analog/digital (A/D) and digital/analog (D/A) converters [1]-[4]. However, accuracies of these data conversion ICs are usually limited by parasitical effects and low tolerance and fabrication yield in the GaAs FET technologies. Global and local deviations have been used to characterize the tolerance of transistors and other passive elements, where the local deviation (mismatch) within chips represents a critical factor in analysis and design of the precise data conversion circuits [5]-[8]. Based on the Raytheon transistor model, model parameters and their deviations of GaAs E/D HEMTs are measured in this paper, and then analytical characterization with seven model parameters are presented for transistor current sources and differential amplifiers. Monte-carlo simulations are carried out on an 8 bit D/A converter and a latched comparator implemented in the 0.5  $\mu\text{m}$  GaAs E/D HEMT technology, and predicted accuracies are also compared with measured data.

## Transistor Parameters

The Raytheon transistor model [9] was originally developed for GaAs MESFETs and it has been successfully applied for model parameter extraction with HP-TECAP [10] and circuit simulation with HSPICE [11]. This model was also demonstrated to be suitable for a characteristic description of GaAs HEMTs [12],[13]. In this paper, GaAs E/D HEMTs with gate widths of 5  $\mu\text{m}$ , 10  $\mu\text{m}$ , 20  $\mu\text{m}$  and 50  $\mu\text{m}$  and gate lengths of 0.5  $\mu\text{m}$ , 1.0  $\mu\text{m}$  and 2.0  $\mu\text{m}$  are measured on three wafers and their model parameters are extracted with HP-TECAP based on the Raytheon model. 500  $\mu\text{m}$  gate width transistors are also measured to determine the capacitance parameters of the model. 14 model parameters are extracted, but only seven parameters of them are selected for the circuit characterization, because static accuracy of analog circuits is determined by these seven parameters as described below. These seven parameters are drain current parameters  $V_{T0}$ ,  $\beta$ ,  $b$ ,  $\alpha$  and  $\lambda$ , and parasitical resistances  $R_d$  and  $R_s$ . As an example, Fig.1 and Fig.2 show measured parameters  $V_{T0}$  and  $\beta$  and their deviations as functions of gate width  $W_g$ , gate length  $L_g$  and distance  $D$  between transistors.

According to the measured data, the parameter deviations with various gate widths, gate lengths and distances are calculated by the empirical formula:

$$\sigma^2(x_i) = \frac{P_W^2(x_i)}{W_g^2} + \frac{P_L^2(x_i)}{L_g^2} + P_D^2(x_i) D^2, \quad (1)$$

where  $x_i$ ,  $i \in 1-7$ , represent the seven model parameters. The factors  $P_W$ ,  $P_L$ , and  $P_D$  are determined and given in Table 1. Correlations between two parameters  $x_i$  and  $x_j$  will be described by the correlation coefficient  $\rho(x_i, x_j)$

$$\rho(x_i, x_j) = \frac{\frac{1}{n_z} \sum_{k=1}^{n_z} [x_i(k) - \bar{x}_i] [x_j(k) - \bar{x}_j]}{\sigma(x_i) \sigma(x_j)}, \quad (2)$$

where  $n_z$  is the number of measured transistors,  $x_i$  and  $x_j$



and  $\sigma(x_i)$  and  $\sigma(x_j)$  are the average values and the standard deviations of the parameters  $x_i$  and  $x_j$ , respectively. The determined correlation coefficients of the depletion and enhancement HEMTs are listed in Table 2.

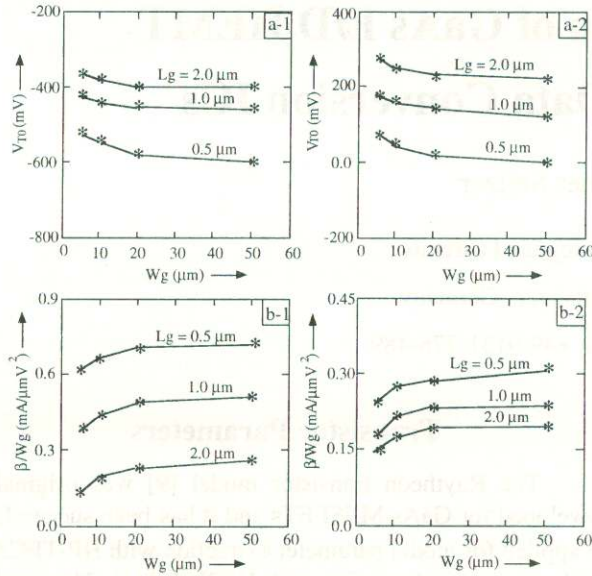


Fig.1: GaAs E/D HEMT model parameters  $V$  versus gate width  $W_g$  and gate length  $L_g$ .

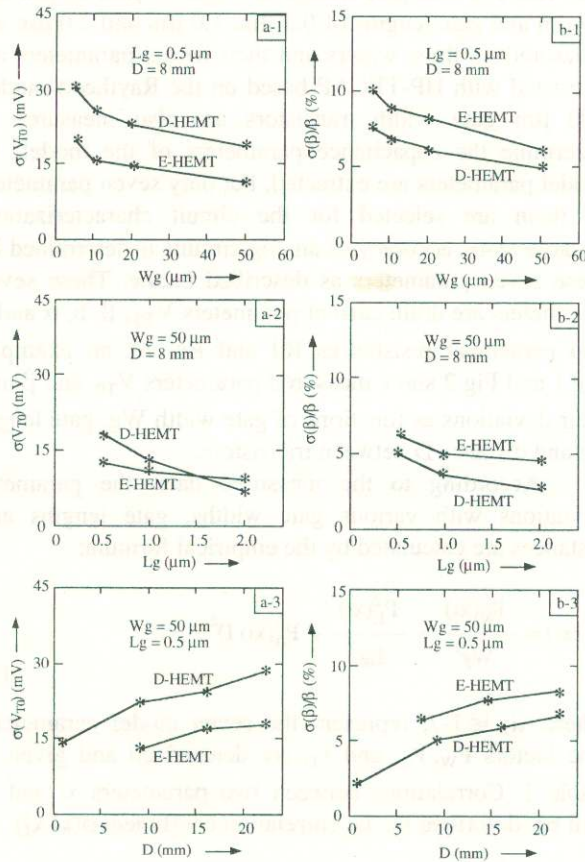


Fig.2: Model parameter deviations versus gate width  $W_g$ , gate length  $L_g$  and distance  $D$ .

Transistor	Parameter	$V_{T0}$	$\beta$	$b$	$\alpha$	$\lambda$	$R_d$	$R_s$
D-HEMT	$P_W$ (% $\mu m$ )	22,4	28,3	78,1	14,4	92,5	25,3	16,3
	$P_L$ (% $\mu m$ )	1,32	2,13	4,72	0,51	6,34	j0,33	0,78
	$P_D$ (%/mm)	0,19	0,28	0,69	0,27	0,86	0,20	0,28
E-HEMT	$P_W$ (% $\mu m$ )	261,2	37,7	74,0	10,3	73,5	44,7	44,6
	$P_L$ (% $\mu m$ )	19,1	2,43	2,48	0,69	2,80	1,26	1,04
	$P_D$ (%/mm)	2,22	0,31	0,49	0,21	0,58	0,23	0,26

Table 1: Model parameter deviation factors  $P_W$ ,  $P_L$  and  $P_D$ .

Transistor	Parameter	$V_{T0}$	$\beta$	$b$	$\alpha$	$\lambda$	$R_d$	$R_s$
D-HEMT	$V_{T0}$	1,00						
	$\beta$	0,56	1,00					
	$b$	0,75	0,59	1,00				
	$\alpha$	0,12	0,42	0,23	1,00			
	$\lambda$	-0,10	-0,67	-0,26	-0,06	1,00		
	$R_d$	0,40	-0,20	0,44	-0,49	0,08	1,00	
	$R_s$	0,10	-0,25	0,24	-0,12	0,29	0,37	1,00
E-HEMT	$V_{T0}$	1,00						
	$\beta$	0,26	1,00					
	$b$	0,69	0,87	1,00				
	$\alpha$	-0,28	0,43	-0,11	1,00			
	$\lambda$	-0,24	-0,79	-0,47	-0,38	1,00		
	$R_d$	0,32	-0,08	0,41	-0,49	-0,53	1,00	
	$R_s$	0,22	-0,16	0,33	-0,06	0,39	0,43	1,00

Table 2: Correlation coefficients of the model parameters.

## Analytical Characterization

Transistor current sources and differential amplifiers represent two critical components in data conversion ICs, because output current mismatch of the current sources and DC offset voltage of the differential amplifiers are basic limitations of the accuracies of A/D and D/A converters. Therefore, analytical equations are derived for the characterization of these components. For the transistor current sources the output current mismatch is expressed as:

$$\left[ \frac{\sigma(I_{ds})}{I_{ds}} \right]^2 = \sum_{i=1}^7 \sum_{j=1}^7 \frac{\partial I_{ds}}{\partial x_i} \frac{\partial I_{ds}}{\partial x_j} \frac{\rho(x_i, x_j) \sigma(x_i) \sigma(x_j)}{I_{ds}^2} = \sum_{i=1}^7 \sum_{j=1}^7 F_{xi} F_{xj} \rho(x_i, x_j) \left[ \frac{\sigma(x_i)}{x_i} \right] \left[ \frac{\sigma(x_j)}{x_j} \right], \quad (3)$$

where current error functions  $F_{xi}$  and  $F_{xj}$  are:

$$F_{V_{T0}} = \frac{-[2 + b(V_{gs} - V_{T0})] V_{T0}}{[1 + b(V_{gs} - V_{T0})] (V_{gs} - V_{T0}) (1 + g_m R_s)}, \quad (4)$$

$$F_{\beta} = \frac{1}{1 + g_m R_s}, \quad (5)$$

$$F_b = \frac{-b(V_{gs} - V_{T0})}{1 + b(V_{gs} - V_{T0}) (1 + g_m R_s)}, \quad (6)$$



$$F_{\alpha} = \frac{2\alpha V_{ds}}{\sinh(2\alpha V_{ds})(1 + g_m R_s)}, \quad (7)$$

$$F_{\lambda} = \frac{ds}{(1 + \lambda V_{ds})(1 + g_m R_s)}, \quad (8)$$

$$F_{Rd} = \frac{g_{sd} R_d}{1 + g_m R_s}, \quad (9)$$

$$F_{Rs} = \frac{g_m R_s}{(1 + g_m R_s)^2}. \quad (10)$$

The DC offset voltage of a simple differential amplifier with passive load (P.L.) is derived as:

$$\Delta V_{DC}(P.L.) = \sum_{i=1}^8 \sum_{j=1}^8 E_{xi} E_{xj} \rho(x_i, x_j) \left[ \frac{\Delta x_i}{x_i} - \left[ \frac{\Delta x_j}{x_j} \right] \right]. \quad (11)$$

The voltage error functions  $E_{xi}$  and  $E_{xj}$  in this equation are written in equations (12)-(18), and  $R$  is the load resistor,  $I_{ds}$  is the transistor drain current of differential pair and its deviation is calculated by equation (3). Predicted results using the measured parameters and deviations are illustrated in Fig.3 and Fig.4.

$$E_{V_{T0}} = V_{T01,2}, \quad (12)$$

$$E_{\beta} = E_R = - \frac{(V_{gs1,2} - V_{T01,2})[1 + b_{1,2}(V_{gs1,2} - V_{T01,2})]}{2 + b_{1,2}(V_{gs1,2} - V_{T01,2})}, \quad (13)$$

$$E_b = \frac{b_{1,2}(V_{gs1,2} - V_{T01,2})^2}{2 + b_{1,2}(V_{gs1,2} - V_{T01,2})}, \quad (14)$$

$$E_{\lambda} = E_{\beta} \frac{\lambda_{1,2} V_{ds1,2}}{1 + \lambda_{1,2} V_{ds1,2}}, \quad (15)$$

$$E_{Rd} = 0.5 E_{\lambda} \frac{I_{ds1,2} (R_{d1,2} + R_{s1,2})}{V_{ds1,2}}, \quad (16)$$

$$E_{Rs} = E_{Rd} + I_{ds1,2} R_{s1,2}, \quad (17)$$

$$E_{I_{ds}} = I_{ds1,2} R_{s1,2}, \quad (18)$$

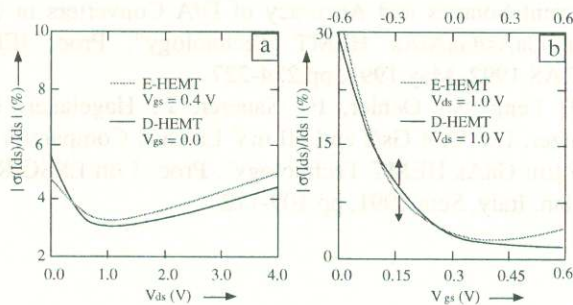


Fig.3: Output current deviations of GaAs E/D HEMT current sources versus bias voltages  $V_{ds}$  and  $V_{gs}$ .

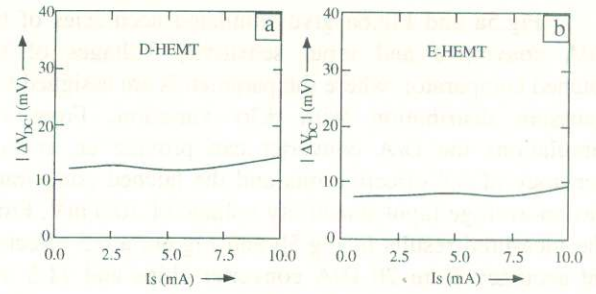


Fig.4: DC offset voltages of GaAs E/D HEMT differential amplifiers with passive loads versus current value  $I_s$  of current sink.

The D-HEMT current sources can achieve the minimum mismatch of 3.0% and the DC offset voltage of the amplifiers with E-HEMT differential pair and passive loads can be reduced into 8.0 mV. The results can be translated to be a 6.0 effective bit accuracy limitation of D/A converters and A/D converters based on fully parallel circuitry.

### Monte-Carlo Simulation

For a Monte-carlo simulation in HSPICE, a model library has been written using the measured parameters and their deviations. Two data conversion ICs that were implemented in the 0.5  $\mu\text{m}$  GaAs E/D HEMT technology are simulated. The first one is an 8 bit D/A converter with differential R-2R weighted network and 8 resistor feedback current sources, which were shown to provide an improved matching ( $\leq 1.2\%$ ) [12]. The second circuit is a latched comparator with preamplifier and SCFL master-slave flip-flops [13].

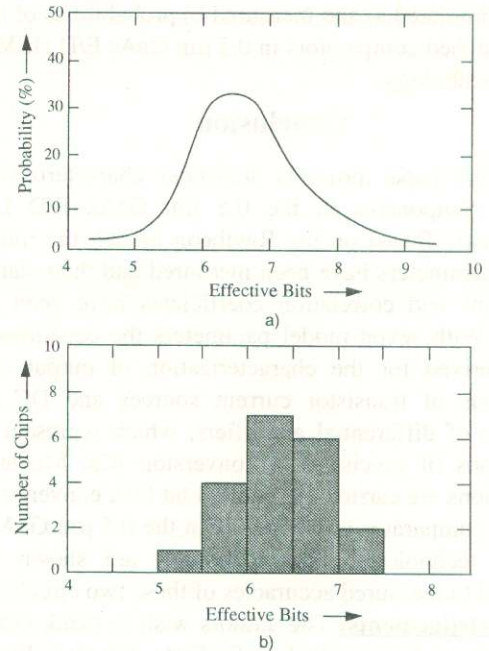


Fig.5: Simulated a) and measured b) probabilities of the 8 bit D/A converters in 0.5  $\mu\text{m}$  GaAs E/D HEMT technology.



Fig.5a and Fig.6a give simulated accuracies of the D/A converters and input sensitivity voltages of the latched comparator, where the parameters are assigned to a gaussian distribution with  $\pm 3\sigma$  variation. From the simulations the D/A converter can provide an average accuracy of 6.8 effective bits and the latched comparator has an average input sensitivity voltage of 10.0 mV. From the measured results in Fig.5b and Fig.6b, a 6.5 effective bit accuracy from 20 D/A converter chips and 11.5 mV input sensitivity voltage from 38 latched comparator chips have been demonstrated.

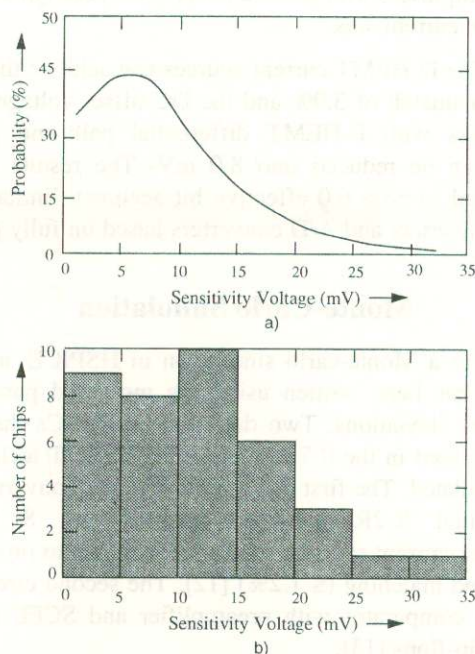


Fig.6: Simulated a) and measured b) probabilities of the latched comparators in 0.5  $\mu\text{m}$  GaAs E/D HEMT technology.

### Conclusion

This paper presents statistical characterization of analog components in the 0.5  $\mu\text{m}$  GaAs E/D HEMT technology. Based on the Raytheon model, the transistor model parameters have been measured and their statistical deviations and correlation coefficients have been determined. With seven model parameters the equations have been derived for the characterization of output current deviations of transistor current sources and DC offset voltages of differential amplifiers, which represent basic limitations of precise data conversion ICs. Monte-carlo simulations are carried out on an 8 bit D/A converter and a latched comparator implemented in the 0.5  $\mu\text{m}$  GaAs E/D HEMT technology. The predictions are shown to be identical to measured accuracies of these two circuits.

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